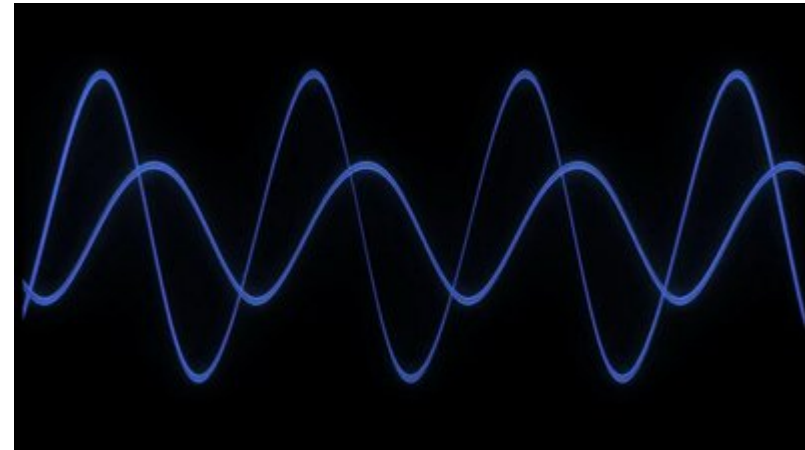


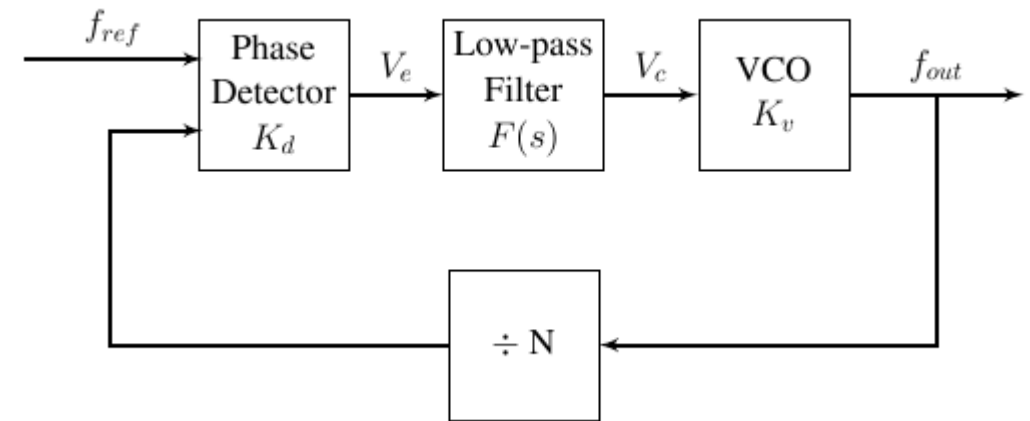
Design of VCOs in Global Foundries 28 nm HPP CMOS

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33rd Annual Microelectronics Conference
Rochester Institute of Technology
Department of Electrical and Microelectronic Engineering
May 12, 2015

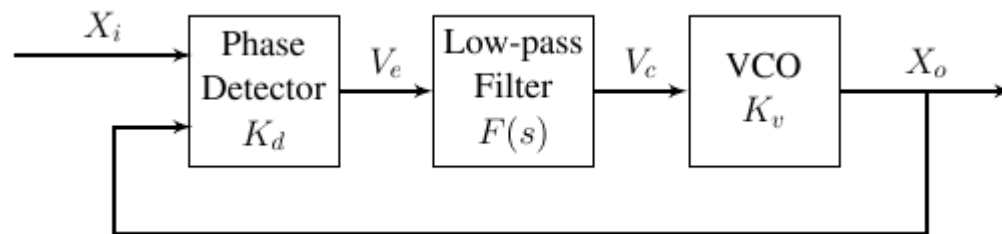
- I. Motivation
- II. Contributions of this work
- III. VCO Theory
 - I. General
 - II. VCO Characteristics
 - III. Ring Oscillators
 - IV. LCVCOs
- IV. VCO Topologies
 - I. Ring Oscillators
 - II. LCVCOs
- V. Design Method
 - I. Ring Oscillators
 - II. LCVCOs
- VI. Results
 - I. Ring Oscillators
 - II. LCVCOs
 - III. Physical Design
- VII. Conclusions



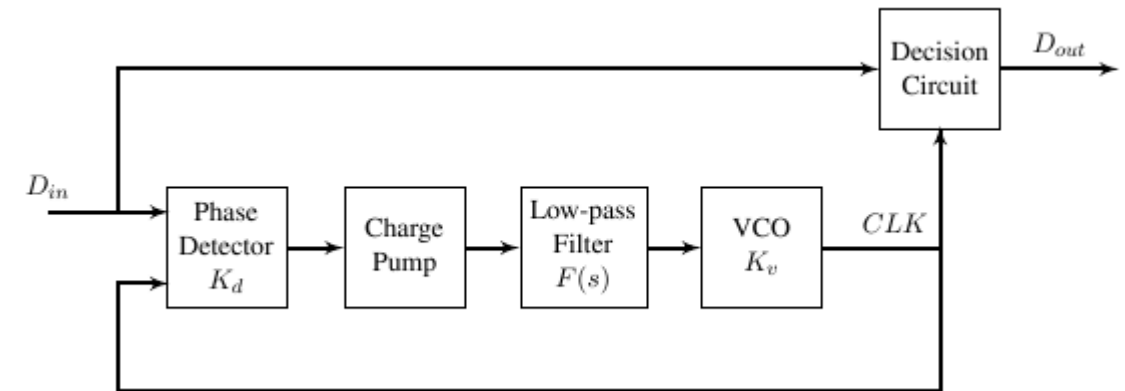
- Demand for faster and lower power communications networks and devices is increasing
 - SoCs being designed in more scaled technologies
 - Current demands require PLL in GHz range
 - Frequency synthesis for clock generation
 - Clock and data recovery (CDR) for high speed IOs
 - Frequency modulation and demodulation
 - VCOs are a core block in PLLs
- Design challenges in deep sub-micron
 - Lower supply voltage (sub 1 V)
 - Worse short-channel effects
 - Higher process variation
 - More influence from parasitics
 - Higher flicker and thermal noise



Frequency synthesizer

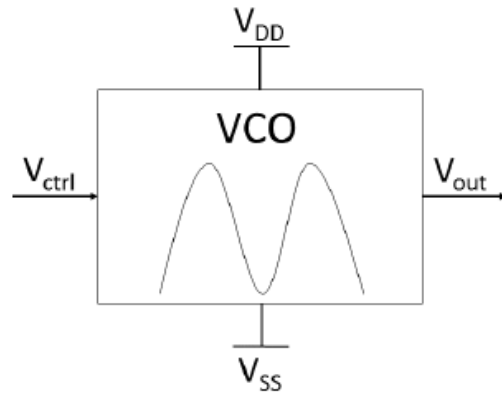


Basic PLL



CDR circuit

1. MATLAB model for predicting center frequency and phase noise of single-ended ring oscillators
2. MATLAB model for design of NMOS-only and self-biased CMOS LCVCOs
3. Case study showing disadvantages of using an LDO for tuning and regulation of ring oscillators in deep sub-micron technology
4. New digital tuning method for LCVCOs
5. Detailed performance comparison of ring oscillators and LCVCOs in a deep sub-micron technology
6. Test chip in GlobalFoundries 28 nm HPP CMOS process



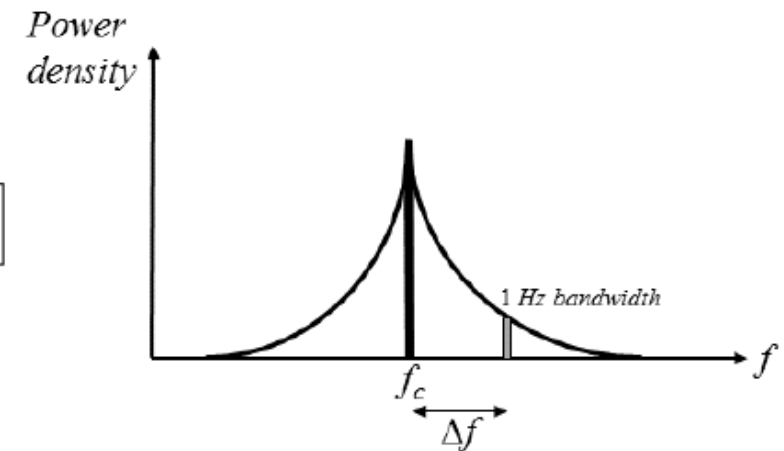
Basic VCO block diagram

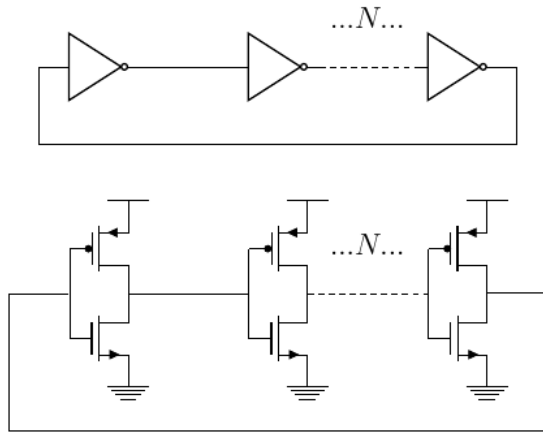
VCO frequency $f_{VCO} = f_0 + K_{VCO}V_{ctrl}$

VCO gain $K_{VCO} = \frac{\delta f_c}{\delta V_{ctrl}}$

- VCO characteristics
 - Center frequency and tuning range
 - Center frequency is frequency in middle range of V_{ctrl}
 - LCVCO generally has higher center frequency
 - Tuning range is range of frequency around center
 - Ring VCO generally has greater tuning range
 - Power consumption and area
 - LCVCO has higher power consumption and area
 - Mostly due to size of integrated inductor
 - Manufacturability
 - LCVCO is harder to integrate into some processes due to integrated inductor
 - Phase noise
 - Phase noise is jitter in frequency domain seen as sideband noise power around center frequency
 - LCVCO generally has lower phase noise

$$\mathcal{L}(f_c, \Delta f) = 10 \cdot \log \left[\frac{P_{sideband}(f_c + \Delta f, 1Hz)}{P_{carrier}} \right]$$





Single-ended ring oscillator

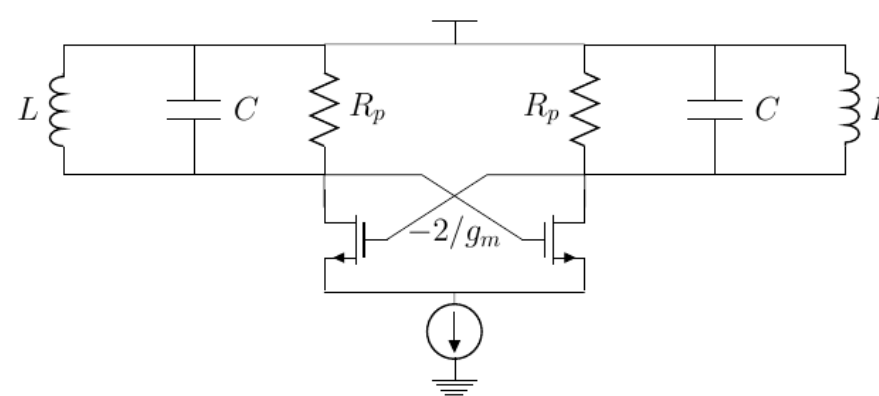
Center frequency $f_0 = \frac{1}{2N \cdot t_d}$ $t_d = \eta R_{DSeff} C_L$

$$R_{DSeff} = \frac{\frac{1}{\beta_n(V_{DD}-V_{tn})} + \frac{1}{\beta_p(V_{DD}-V_{tp})}}{2} \quad C_L = C_{in} + C_{para}$$

Phase noise of ring VCO $L\{f_c, \Delta f\} = \frac{8}{3\eta} \frac{kT}{P} \frac{V_{DD}}{V_{char}} \frac{f_c^2}{\Delta f^2}$

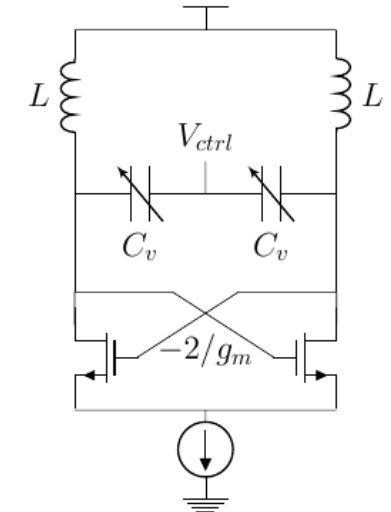
$$P = 2\eta N V_{DD} q_{max} f_0 \quad V_{char} = \frac{E_c L}{\gamma}$$

E_c related to v_{sat} and μ_{eff} from SCM



LC oscillator with cross-coupled differential pair

Negative resistance $-2/g_m$ must be equivalent to parasitic tank resistance $2R_p$

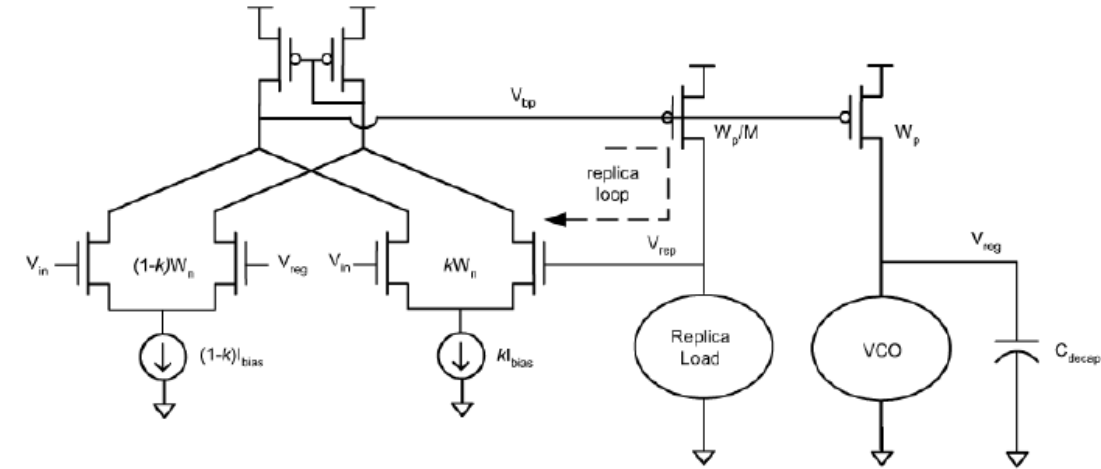


LC voltage-controlled oscillator with cross-coupled differential pair

Center frequency $\omega_0 = \frac{1}{\sqrt{LC}}$ or $f_0 = \frac{1}{2\pi\sqrt{LC}}$

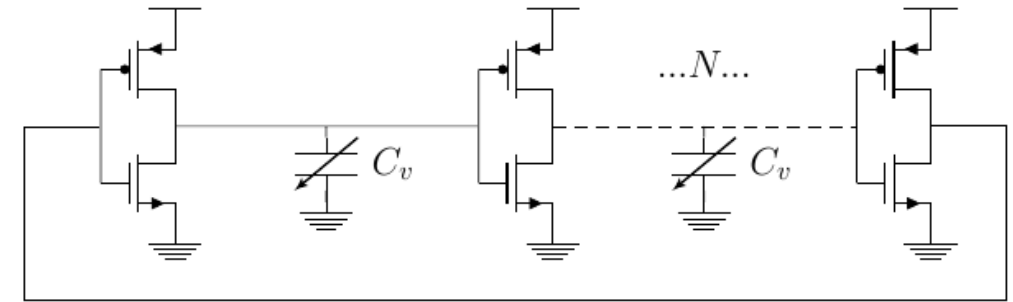
Phase noise of LCVCO $\mathcal{L}\{\Delta f\} = \frac{1}{8\pi^2 f_{off}^2} \cdot \frac{1}{V_0^2 C_{tank}^2} \cdot \sum_n \left(\frac{\overline{i_n^2}}{\Delta f} \cdot \Gamma_{rms,n}^2 \right)$

- Five ring oscillators of 5, 7, 9, 11, and 15 stages (with no LDO) were designed and simulated to check accuracy of frequency prediction model versus simulation results
- Three 5 GHz ring VCO systems were designed and simulated for a case study of LDO versus no LDO
 - VCO1 is a 7 stage LDO regulated ring VCO
 - With LDO using thin oxide devices and a 0.85 V supply
 - Supply across ring oscillator delay stages is reduced by roughly 0.15 V due to drop across regulator
 - VCO2 is a 15 stage LDO regulated ring VCO
 - With LDO using medium oxide devices and a 1.5 V supply
 - Enables full 0.85 V across the ring oscillator delay stages
 - VCO3 is 11 stage varactor-tuned ring VCO with 0.85 V supply and no LDO



Low dropout regulator (LDO) tuned ring VCO

- Advantages
 - Good power supply noise rejection
- Disadvantages
 - More power consumption and area
 - Limited output swing
 - More noise sources contributing to phase noise

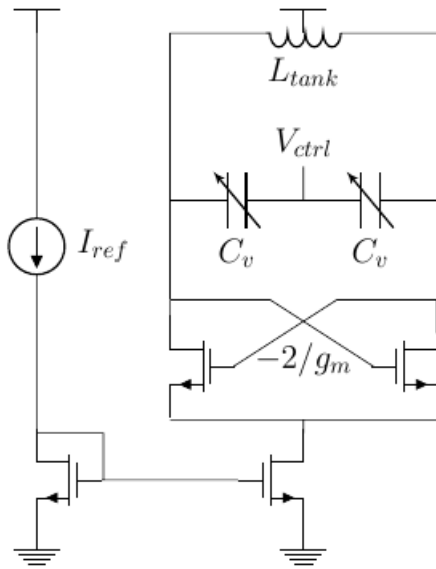


Varactor-tuned ring VCO

- Advantages
 - Less power consumption and area
 - Output swing up to V_{DD}
 - Fewer noise sources contributing to phase noise
- Disadvantages
 - Poor power supply noise rejection

Varactor-tuned ring VCO may be more preferable in deep sub-micron technologies

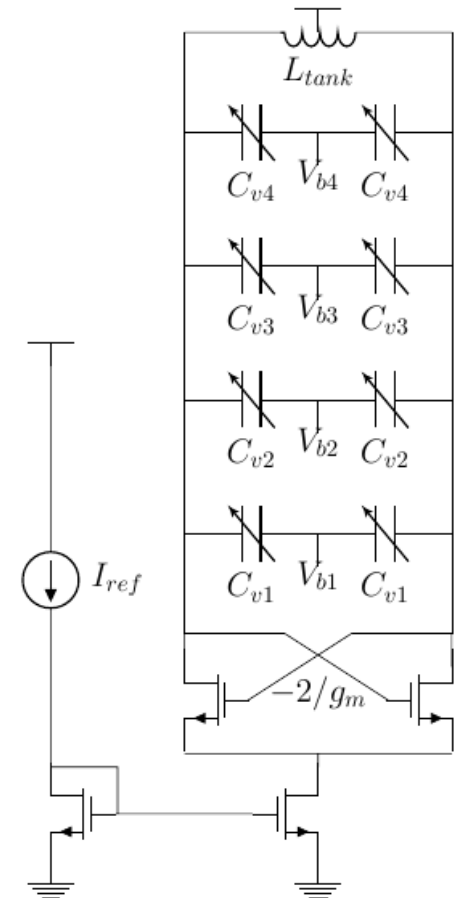
- Four LCVCO were designed
 - 15 GHz Varactor-tuned NMOS-only (VT NMOS)
 - 14.2 GHz Digitally-tuned NMOS-only (DT NMOS)
 - 9 GHz Varactor-tuned self-biased CMOS (VT CMOS)
 - 8.2 GHz Digitally-tuned self-biased CMOS (DT CMOS)
- The varactor-tuned topologies are tuned using one varactor pair receiving V_{ctrl} in range of 0-0.85 V
- The digitally-tuned topologies tuned using four banks of varactor pairs biased at either 0 V or 0.85 V
 - Varactors operate only in min or max capacitance region of C-V curve
 - Increases tuning range and selectivity



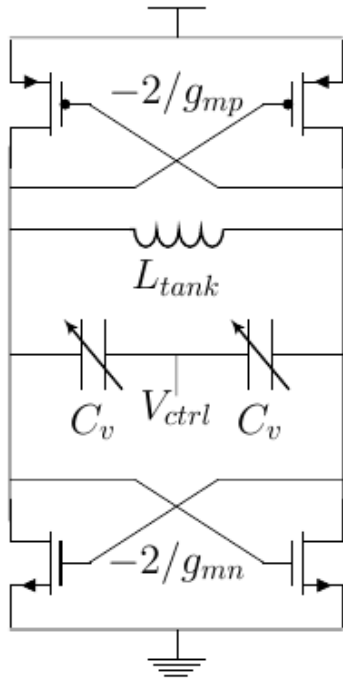
Varactor-tuned NMOS-only LCVCO
(VT NMOS)

- NMOS-only has higher speed
- V_{DD} on inductor enables higher output swing

- Digitally-tuned LCVCO bias scheme:
- Encode 16 capacitance values from 4-bit digital bias
 - Capacitors $C_{v2}=2C_{v1}$, $C_{v3}=4C_{v1}$, and $C_{v4}=8C_{v1}$
 - Controlled through 4-bit external bias voltages V_{b1} , V_{b2} , V_{b3} , and V_{b4} , where V_{b1} is the LSB and V_{b4} the MSB.
 - Bias voltages either 0 V or 0.85 V, making capacitance minimum or maximum.



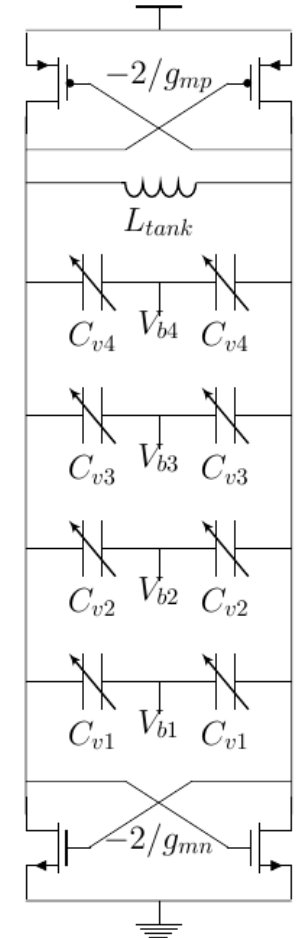
Digitally-tuned NMOS-only LCVCO
(DT NMOS)



Varactor-tuned self-biased
CMOS LCVCO (VT CMOS)

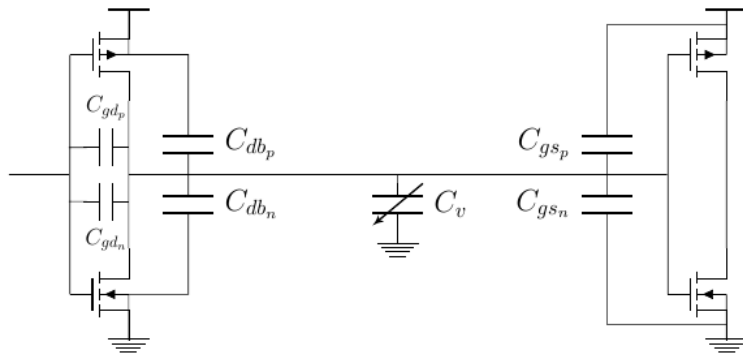
- Removing current source maximizes output swing
- Removes associated noise

- Uses same bias scheme as
Digitally-tuned NMOS LCVCO



Digitally-tuned self-biased
CMOS LCVCO (DT CMOS)

- Design method based on more accurate expression for center frequency
 - Accurate consideration of inter-stage capacitances
 - Effect from gate resistance
- Design variables W_n , W_p , L , V_{DD} , and N are inputs
- Center frequency is output



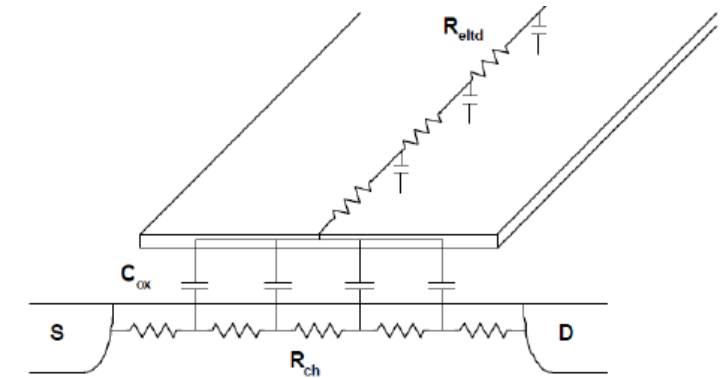
Inter-stage input and parasitic capacitances

$$C_L = C_{in} + C_{para}$$

$$C_{in} = C_{gs_n} + C_{gs_p}$$

$$C_{para} = C_{db_n} + C_{db_p} + C_{gd_n} + C_{gd_p} + C_v$$

- Gate resistance affects circuit through voltage drop across R_g onto C_{in}
- This shifts the time when the output voltage swing crosses midpoint $V_{DD}/2$



Distributed gate resistance

$$R_{sh} = \frac{R_{sh1} R_{sh2}}{R_{sh1} + R_{sh2}}$$

$$R_g = R_{sh} \left(\left(\frac{d_{CG}}{L} \right) + \left(\frac{W_{eff}}{mL} \right) \right)$$

After considering this effect and going through calculations, end up with R_g frequency multiplier term

$$f_0 = \frac{1}{2N \cdot t_d} \left(1 - \frac{R_g C_{para}}{R_{DSeff} (C_{in} + C_{para})} \left(2 - N \left(\frac{1}{2} - \frac{1}{\pi} \right) \right) + \frac{2\sqrt{2}N}{\pi} \right)$$

- Design method based on the following criteria:
 - Frequency and tuning range
 - Tank amplitude constraint
 - Startup condition

Frequency and tuning range

$$\omega = \frac{1}{\sqrt{L_{tank}C_{tank}}} \quad or \quad f = \frac{1}{2\pi\sqrt{L_{tank}C_{tank}}}$$

$$C_{tank} = 0.5 (C_{NMOS} + C_{PMOS} + C_L + C_v + C_{load})$$

$$C_{NMOS} = 4C_{gd_n} + C_{gs_n} + C_{db_n}$$

$$C_{PMOS} = 4C_{gd_p} + C_{gs_p} + C_{db_p}$$

$$\omega_{min} \geq \frac{1}{\sqrt{L_{tank}C_{tank,max}}} \quad \omega_{max} \leq \frac{1}{\sqrt{L_{tank}C_{tank,min}}}$$

Tank amplitude constraint

$$V_{tank,min} = \frac{I_{bias}}{g_{tank,max}}$$

$$g_{tank} = 0.5 (g_{on} + g_{op} + g_v + g_L)$$

$$g_L = \frac{1}{R_p} + \frac{Rs}{\omega^2 L_{ind}^2}$$

$$g_v = \omega^2 C_v^2 R_v$$

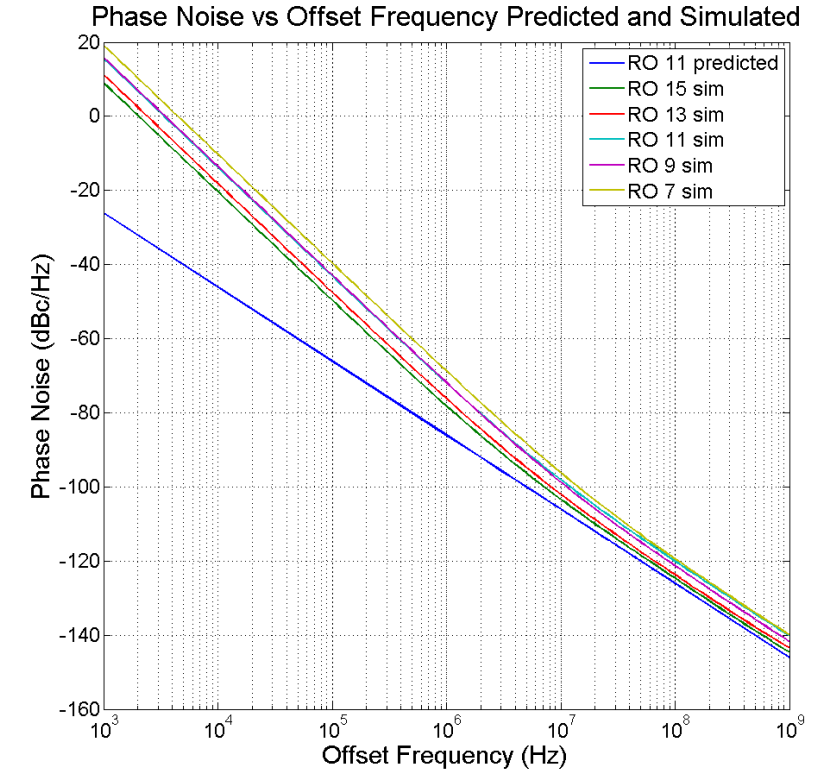
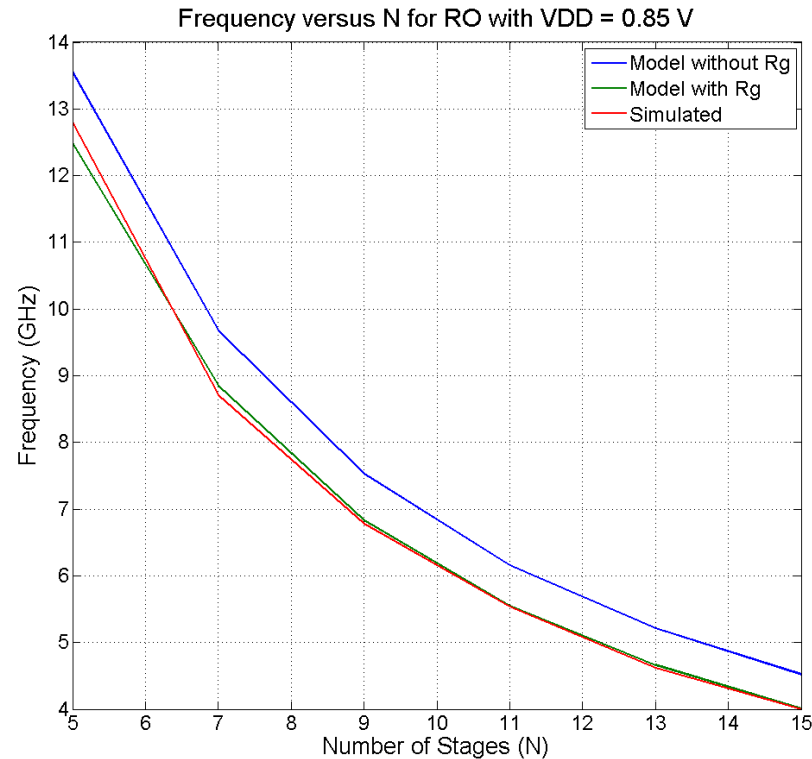
$$g_{tank,max} \text{ occurs at } C_{v,max}$$

Startup condition

$$g_{active} \geq \alpha_{min} g_{tank,max}$$

$$g_{active} = 0.5 (g_{mn} + g_{mp})$$

Expressions for ω_{min} and ω_{max} , $V_{tank,min}$, and g_{active} are solved for $C_{v,max}$ in terms of W_n and plotted in MATLAB over a range of W_n

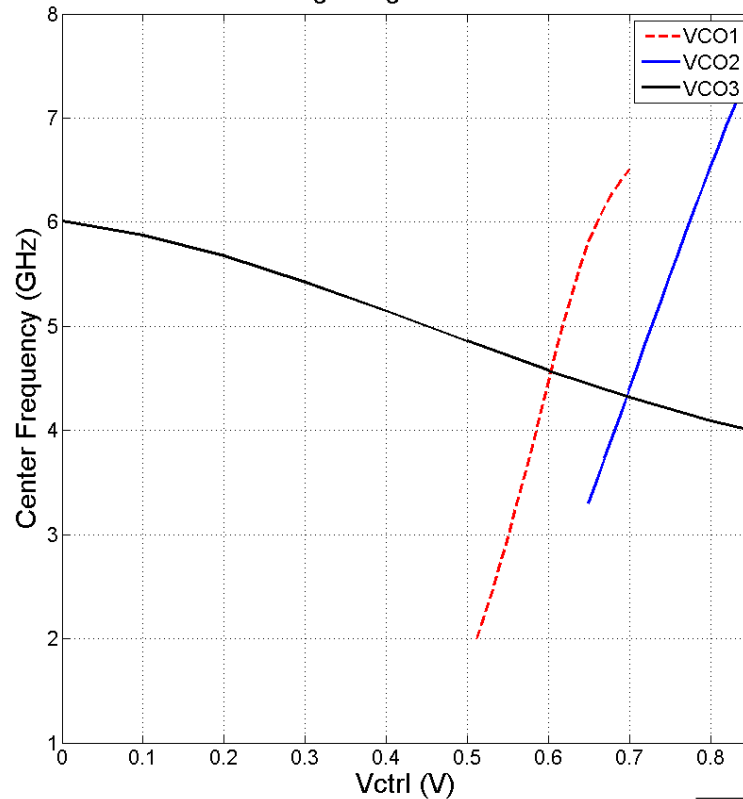


- Ring oscillators of 7, 9, 11, 13 and 15 stages designed and simulated
 - R_g has significant effect on frequency
 - Model without R_g overestimates frequency by about 15%
 - Model with R_g predicts frequency within 1-2%

- Predicted versus simulated phase noise
 - Beyond 1 MHz offset frequency simulated and predicted are close
 - Within 1 MHz simulated is worse than predicted due to flicker noise not being accounted for in expression

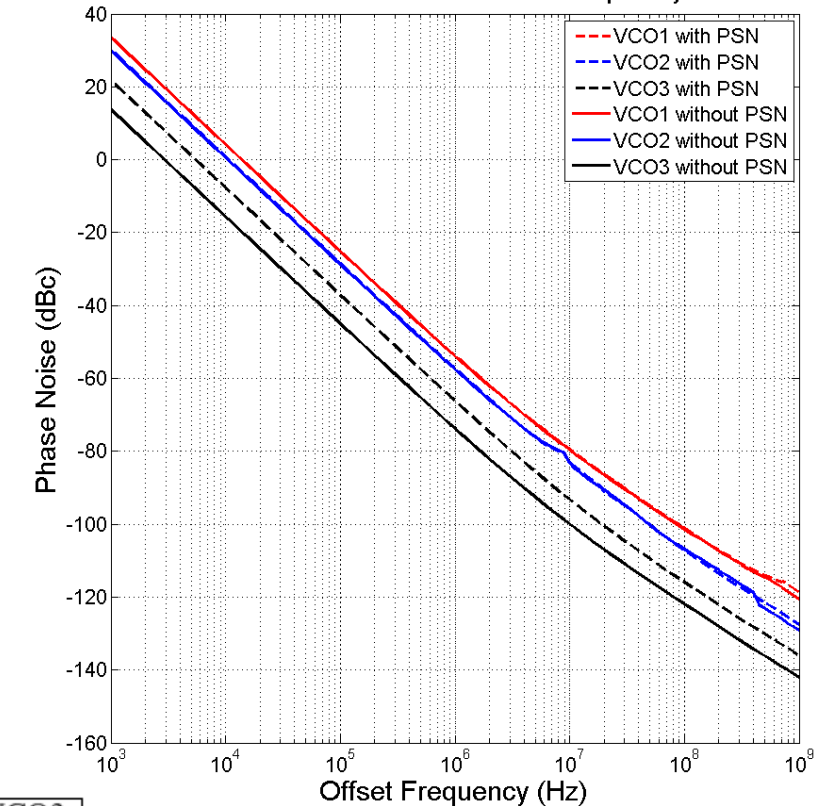
Results: Ring Oscillator LDO Comparison

Tuning Range versus Vctrl

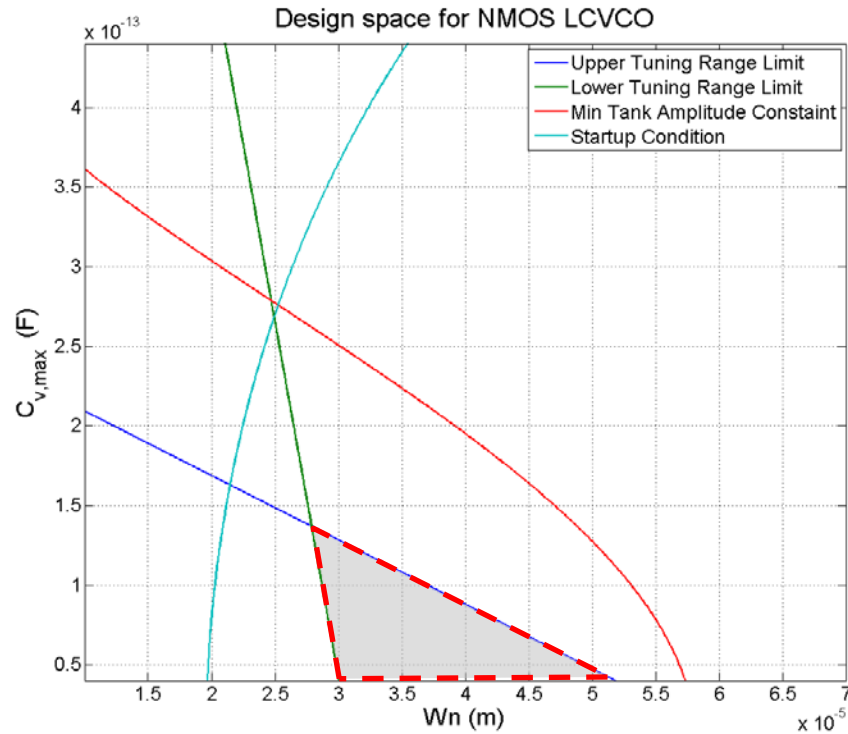


- Tuning range of VCO3 is lower than that of both LDO-tuned VCOs
 - Selectivity of VCO3 is greater
- Phase noise of both LDO-tuned VCOs are nearly the same with and without PSN
 - Shows LDO PSR is working
- Phase noise of VCO3 is significantly lower than VCO1 and VCO2 even with PSN
 - Shows varactor-tuning method may be preferred over LDO-tuning method

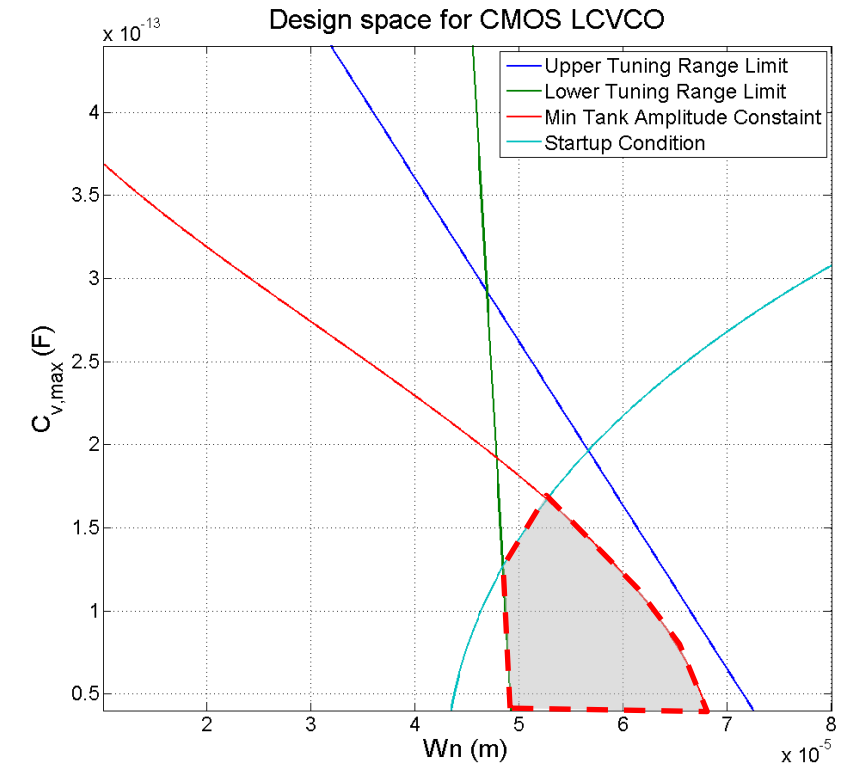
Phase Noise versus Offset Frequency



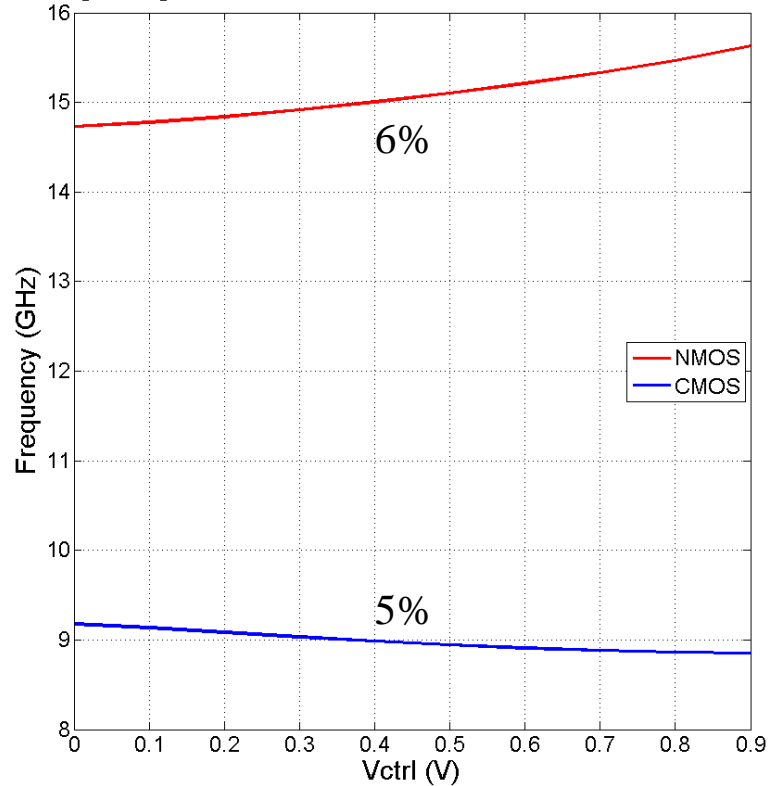
	VCO1	VCO2	VCO3
Tuning Range (%)	90%	80%	40%
Phase Noise (1 MHz) with PSN (dBc/Hz)	-53.79	-57.35	-66.24
Phase Noise (1 MHz) without PSN (dBc/Hz)	-53.96	-57.59	-73.86
P_{avg} (μ W)	77	1940	750
Active area (μ m ²)	311.2	11730	28.6



- Valid design space
 - below upper TR limit
 - above lower TR limit
 - below tank amplitude constraint
 - below startup condition
- Optimize through parametric simulation within valid design space

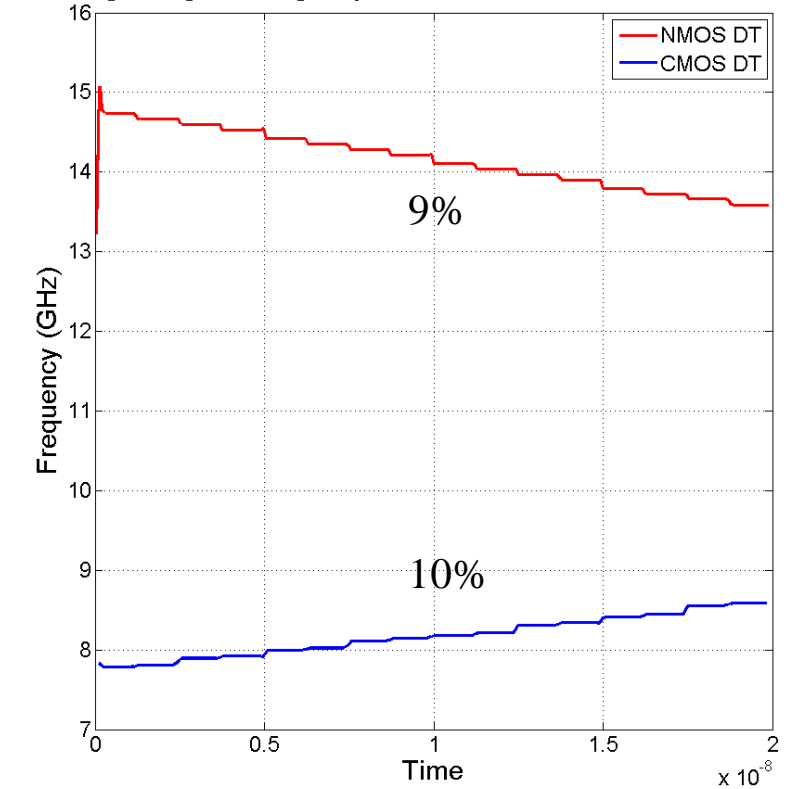


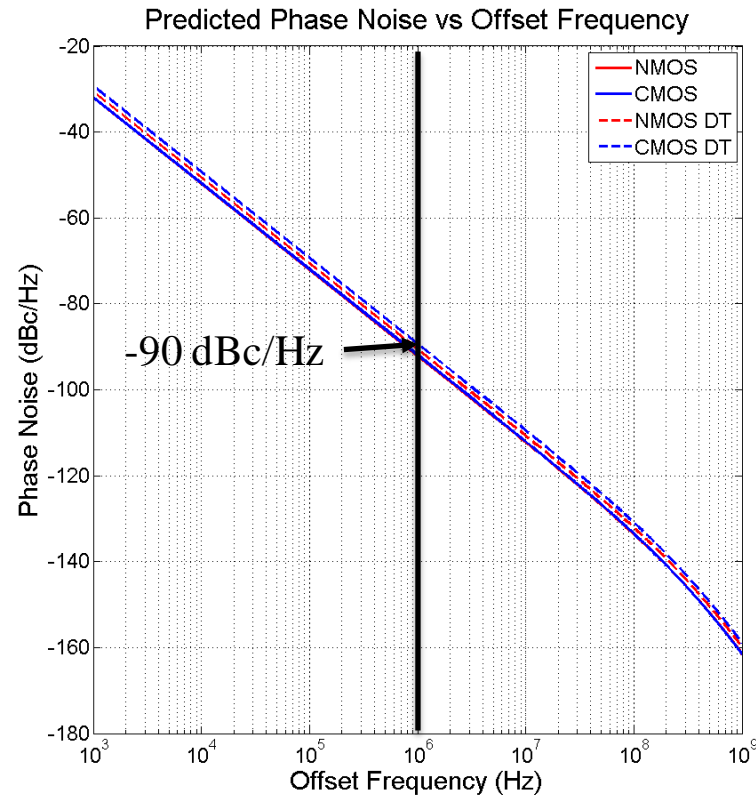
Tuning Range for Varactor Tuned NMOS and CMOS LCVCOs



- Tuning range of digitally-tuned LCVCOs is nearly double that of varactor-tuned
- Frequency tuned in flat steps giving greater selectivity

Tuning Range for Digitally Tuned NMOS and CMOS LCVCOs



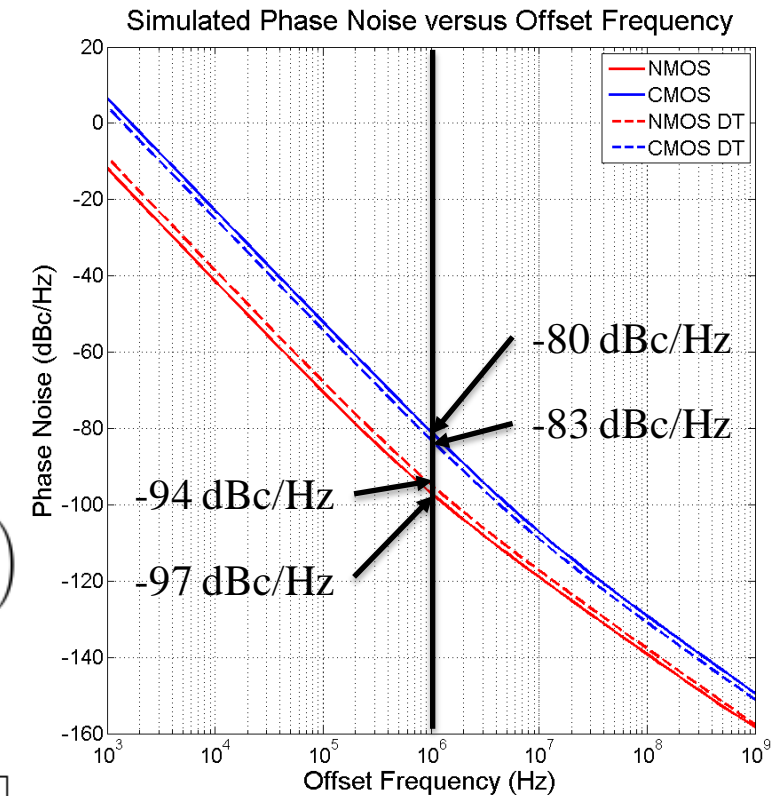


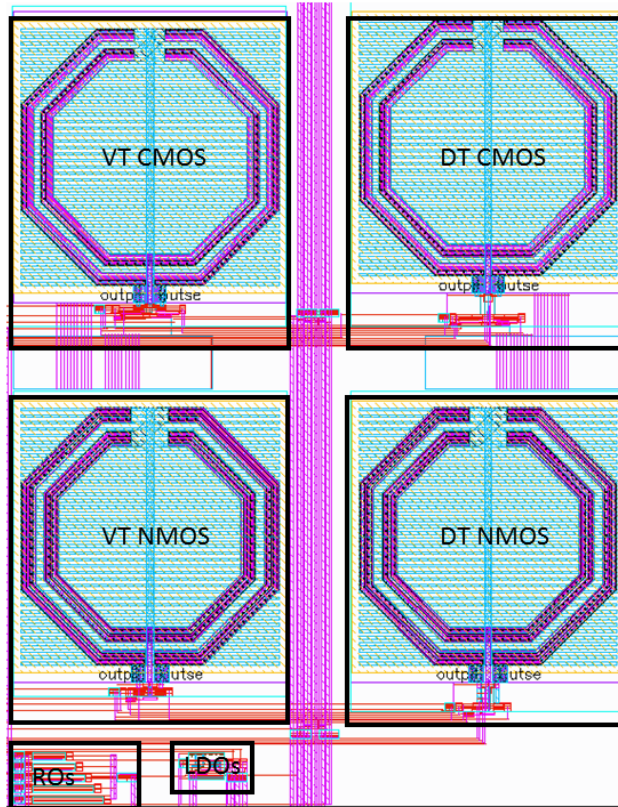
- Phase noise in general is fairly close to predicted
- VT NMOS has best phase noise -97 dBc/Hz at 1 MHz offset
- DT CMOS improves phase noise over VT CMOS by -3 dBc/Hz

$$FOM = \mathcal{L}(f_{off}) - 20 \cdot \log\left(\frac{f_0}{f_{off}}\right) + 10 \cdot \log\left(\frac{P_{DC}}{1mW}\right)$$

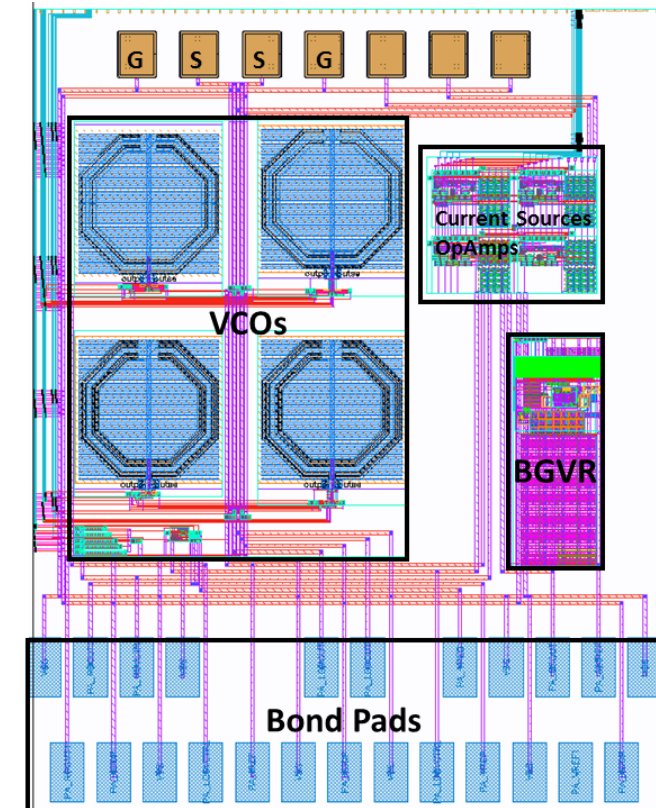
$$FOMT = FOM - 20 \cdot \log\left(\frac{TR}{10}\right)$$

	NMOS	NMOS DT	CMOS	CMOS DT
f_c (GHz)	15	14.2	9	8.2
TR (%)	6	9	5	10
PN 1 MHz (dBc/Hz)	-97	-94	-80	-83
P_{DC} (mW)	6.8	6.8	17	17
FOM (dBc/Hz)	-172.20	-168.72	-146.78	-148.97
FOMT (dBc/Hz)	-167.76	-167.81	-140.76	-148.97





- Octagonal structures are symmetric spiral inductors
- one for each of the 4 LCVCOs
- Output signals from all VCOs are shielded by GND lines



- Output of all LCVCOs goes to RF probe pads through CML buffers
- Output of ring oscillators goes to bondpads through tapered inverter buffers

Ring Oscillators

	VCO1	VCO2	VCO3
Tuning Range (%)	90%	80%	40%
Phase Noise (1 MHz) with PSN (dBc/Hz)	-53.79	-57.35	-66.24
Phase Noise (1 MHz) without PSN (dBc/Hz)	-53.96	-57.59	-73.86
P_{avg} (μ W)	77	1940	750
Active area (μ m ²)	311.2	11730	28.6

- R_g has significant effect on predicting center frequency
 - With inclusion of R_g model is accurate to within 1-2%
- Varactor-tuned ring oscillators are preferred to LDO-tuned ring oscillators

LCVCOs

	NMOS	NMOS DT	CMOS	CMOS DT
f_c (GHz)	15	14.2	9	8.2
TR (%)	6	9	5	10
PN 1 MHz (dBc/Hz)	-97	-94	-80	-83
P_{DC} (mW)	6.8	6.8	17	17
FOM (dBc/Hz)	-172.20	-168.72	-146.78	-148.97
FOMT (dBc/Hz)	-167.76	-167.81	-140.76	-148.97

- VT NMOS LCVCO has overall best phase noise of -97 dBc/Hz at 1 MHz offset
- Digitally-tuned method improves tuning range
 - NMOS LCVCO by 50%
 - CMOS LCVCO by 100%
- Phase noise improved by 3 dBc/Hz with DT CMOS LCVCO

- Design in 14 nm FinFET PDK
- Preliminary results for VCOs designed in 14 nm FinFET
 - Tuning range of LCVCOs in 14 nm FinFET is roughly 2X that of those designed in 28 nm planar CMOS
 - Phase noise of LCVCOs is affected more by V_{ctrl}
- Further work in 14 nm FinFET PDK will continue with other students in research group

- Support through Rambus
 - Anand Gopalan
 - Fred Heaton
 - John Eble
- Fabrication
 - GlobalFoundries
- Thesis Advisor
 - Dr. Mukund
- Thesis Committee Members
 - Dr. Moon
 - Dr. Pearson
- Colleagues
 - Jonathan Zimmermann
 - Sagar Saxena
 - Narendra Mane
 - Lucas Prilenski
 - Srujan Shivanakere
- System administration
 - Jim Stefano
 - Emilio Del Plato
- Assistance with maintaining Cadence tools
 - Mark Indovina